What is claimed is:

[Claim 1] 1. A method of manufacturing an interconnect, comprising:

(a) providing a substrate;

(b) forming a dielectric layer on said substrate;

(c) forming a wire in said dielectric layer, a top surface of said wire coplanar with a top surface of said dielectric layer;

(d) forming a first capping layer on said top surface of said wire and said top surface of said dielectric layer, said first capping layer thin enough to allow penetration of said first capping layer by a point of a conductive probe tip in order to make electrical contact to said wire; and

(e) after step (d) forming a second capping layer on a top surface of said first capping layer.

[Claim 2] 2. The method of claim 1, wherein said wire includes copper exposed to an ambient atmosphere at said top surface of said wire.

[Claim 3] 3. The method of claim 2, wherein said first capping layer is sufficiently thick to prevent formation, on said top surface of said wire, of copper containing particles by reaction of said wire with said dielectric layer.

[Claim 4] 4. The method of claim 1, wherein said dielectric layer comprises fluorinated silicon glass.

[Claim 5] 5. The method of claim 4, wherein said dielectric layer comprises about 1% to about 9% by weight of fluorine.

[Claim 6] 6. The method of claim 4, wherein said wire includes copper exposed to an ambient atmosphere at said top surface of said wire.

[Claim 7] 7. The method of claim 6, wherein said first capping layer is sufficiently thick to prevent formation , on said top surface of said wire, of copper containing particles by reaction of copper in said wire with fluorine in said dielectric layer.

[Claim 8] 8. The method of claim 1, wherein said first capping layer and said second capping layer independently include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 9] 9. The method of claim 1, wherein said first capping layer and said second capping layer independently

include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 10] 10. The method of claim 1, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

[Claim 11] 11. The method of claim 1, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

[Claim 12] 12. The method of claim 1, wherein said second capping layer is a copper diffusion barrier.

[Claim 13] 13. The method of claim 1, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

[Claim 14] 14. The method of claim 1, further including:

(f) forming another dielectric layer on a top surface of said second capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer.

[Claim 15] 15. The method of claim 1, wherein forming said first capping layer comprises forming silicon nitride by high density plasma deposition and forming said second capping layer comprises forming silicon nitride formed by plasma enhanced chemical vapor deposition.

[Claim 16] 16. The method of claim 1, further including between steps (d) and (e), cleaning said top surface of said first capping layer.

[Claim 17] 17. The method of claim 1, further including between steps (d) and (e), cryogenically cleaning said top surface of said first capping layer.

[Claim 18] 18. The method of claim 1, further including between steps (c) and (d), cleaning said top surface of said wire and said top surface of said dielectric layer in a reducing environment.

[Claim 19] 19. The method of claim 1, further including between steps (d) and (e), performing one or more characterization procedures selected from the group consisting of optical or SEM inspection and optical or SEM image size measurement.

[Claim 20] 20. The method of claim 1, wherein said first capping layer is thin enough to be transparent to visible light, to back-scattered electrons in a SEM or to both.

[Claim 21] 21. The method of claim 1, wherein said second capping layer is formed at a temperature of about 350°C or greater.

[Claim 22] 22. A method of manufacturing an integrated circuit, comprising:

(a) providing a substrate;

(b) forming a copper diffusion barrier layer on said substrate;

(c) forming a dielectric layer on a top surface of said copper diffusion barrier layer;

(d) forming a copper damascene or dual damascene wire in said dielectric layer, a top surface of said copper damascene or dual damascene wire coplanar with a top surface of said dielectric layer;

(e) forming a first capping layer on said top surface of said wire and said top surface of said dielectric layer;

(f) after step (e) performing one or more characterization procedures in relation to said integrated circuit; and

(g) after step (f) forming a second capping layer on said top surface of said first capping layer.

[Claim 23] 23. The method of claim 21, wherein said dielectric layer comprises fluorinated silicon glass.

[Claim 24] 24. The method of claim 22, wherein said dielectric layer comprises about 1% to about 9% by weight of fluorine.

[Claim 25] 25. The method of claim 23, wherein said first capping layer is sufficiently thick to prevent formation, on said top surface of said wire, of copper containing particles by reaction of copper in said wire with fluorine in said dielectric layer.

[Claim 26] 26. The method of claim 21, wherein said first capping layer and said second capping layer independently include a material selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 27] 27. The method of claim 21, wherein said first capping layer and said second capping layer independently include one or more layer of materials selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y.

[Claim 28] 28. The method of claim 21, wherein said first capping layer has a thickness between about 100 Å and 300 Å.

[Claim 29] 29. The method of claim 21, wherein said second capping layer has a thickness between about 150 Å and 700 Å.

[Claim 30] 30. The method of claim 21, wherein said second capping layer is a copper diffusion barrier.

[Claim 31] 31. The method of claim 21, wherein said first capping layer in combination with said second capping layer is a copper diffusion barrier.

[Claim 32] 32. The method of claim 21, further including:

(h) forming another dielectric layer subsequently formed on a top surface of said second capping layer, said second capping layer acting as a reactive ion etch stop for etching said another dielectric layer.

[Claim 33] 33. The method of claim 21, wherein forming said first capping layer comprises forming silicon nitride by high density plasma deposition and forming said second capping layer comprises forming silicon nitride by plasma enhanced chemical vapor deposition.

[Claim 34] 34. The method of claim 21, further including between steps (f) and (g), cryogenically cleaning said top surface of said first capping layer.

[Claim 35] 35. The method of claim 21, further including between steps (d) and (e), cleaning said top surface of said